Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application.

Listing of Claims

1. (canceled)

2. (currently amended) The method of claim ~~1~~ 7 wherein the control bit is set by a programmer.

3. (currently amended) The method of claim ~~1~~ 7 further comprising:
handling the output signal as an STS connection when the control bit is set.

4. (currently amended) The method of claim ~~1~~ 7 further comprising:
assembling the output signal from multiple VT/TU connections when the control bit is not set.

5. (currently amended) The method of claim ~~1~~ 7 further comprising:
handling the output signal as ~~an~~ the AU connection when the control bit is not set.

6. (currently amended) The method of claim ~~1~~ 7 further comprising:
assembling the output signal from multiple VT connections when the control bit is set.

7. (currently amended) ~~The method of claim 1 further comprising~~: A method of processing an output signal comprising:
checking a state of a control bit that specifies whether to assemble the output signal from multiple virtual tributary (VT) or tributary unit (TU) connections or handle the output signal as an synchronous transport signal (STS) or administrative unit (AU) connection;
switching a predetermined number of entries together based on the state of the control bit; and
storing the control bit in a connection memory.

8. (currently amended) The method of claim ~~1~~ 7 further comprising storing the control bit in a register.

9. (currently amended) The method of claim ~~1~~ 7 further comprising:

checking a state of a second control bit.

10. (original) The method of claim 9 wherein the second control bit is associated with independent and concatenated payloads.

11. (original) The method of claim 9 further comprising:

cross-connecting a second payload with a first payload if the second control bit is set.

12. (original) The method of claim 9 further comprising:

cross-connecting a second payload with a first payload if the second control bit is not set.

13. (original) The method of claim 9 further comprising storing the second control bit in a connection memory.

14. (original) The method of claim 9 further comprising storing the second control bit in a register.

15. (currently amended) The method of claim 9 further comprising:

checking the second control bit only if the ~~first~~ control bit is set.

16. (canceled)

17. (currently amended) The computer program product of claim ~~16~~ 18 wherein the control bit is set by a programmer.

18. (currently amended) ~~The computer program product of claim 16 further comprising instructions to:~~ A computer program product tangibly embodied on a computer readable medium, for provisioning cross-connects in an output signal in network switching environment comprising instructions for causing a computer to:

check a state of a control bit that specifies whether to assemble the output signal from multiple virtual tributary/tributary unit (VT/TU) connections or handle the output signal as an synchronous transport signal (STS) or administrative unit (AU) connection;

switch a predetermined number of entries together based on the state of the control bit; and

store the control bit in a connection memory.

19. (currently amended) The computer program product of claim ~~16~~ 18 further comprising instructions to store the control bit in a register.

20. (currently amended) The computer program product of claim ~~16~~ 18 further comprising instructions to:

check a state of a second control bit that is associated with independent and concatenated payloads.

21. (previously presented) The computer program product of claim 20 further comprising instructions to store the second control bit in a connection memory.

22. (previously presented) The computer program product of claim 20 further comprising instructions to store the second control bit in a register.

23. (currently amended) The computer program product of claim 20 further comprising instructions to:

check the second control bit only if the ~~first~~ control bit is set.

24. (currently amended) Apparatus for processing an output signal comprising:

a first memory ~~including~~ storing a control bit that specifies whether to assemble ~~an~~ the output signal from multiple virtual tributary (VT) connections or handle the output signal as an synchronous transport signal (STS) or administrative unit (AU) connection;

a circuit to check a state of the control bit; and

control circuitry that uses a second memory to switch a predetermined number of entries together based on the state of the control bit.

25. (previously presented) The apparatus of claim 24 wherein the control circuitry is configured to handle the output signal as an STS connection when the control bit is set.

26. (previously presented) The apparatus of claim 25 wherein the control circuitry is configured to assemble the output signal from multiple VT connections when the control bit is not set.

27. (currently amended) The apparatus of claim 24 wherein the first memory ~~includes~~ stores a second control bit that specifies whether payloads are independent or concatenated, and the control circuit is configured to switch a predetermined number of payloads together based on a state of the second control bit.